

REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 55, 57, 58, 60-62 and 66-80 are pending; Claims 1-54, 56, 59 and 63-65 have been canceled. No new matter is believed to have been added.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 55 and 57, 58, 60-62 and 66-68

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As previously presented, independent Claim 55 is recited below:

55. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to

said second metal pad through an opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a titanium-containing layer between said second metal pad and said copper pillar, wherein said titanium-containing layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad;

a nickel-containing layer between said copper pillar and said solder metal;
and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

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Reconsiderations of Claims 55, 57, 58, 60-62 and 66-68 rejected under 35 U.S.C. .

103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 55 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that Nozawa teaches "a substrate [1000] comprising a solder mask [106] and a first pad [104]". ~ See lines 7-10 on page 3, in the last Office Action mailed Dec. 19, 2008 ~

Applicants respectfully traverse the Examiner's opinion because the element [1000] in Nozawa's device is not a semiconductor chip, but a circuit board. ~ See col. 8, lines 30-44 ~ The elements 106 and 104 are taught not to be arranged on a circuit board, but to be arranged on a semiconductor chip 100. ~ See col. 4, lines 33-39 ~ It is believed that

Nozawa fails to disclose that the circuit board 1000 comprises an electrode 104 and an insulating layer 106 that are formed on a semiconductor chip 100.

Furthermore, Nozawa fails to teach, hint or suggest that a substrate has a first side and a second side opposite to the first side, wherein the substrate comprises multiple contact points at the second side, a solder mask at the first side, an interconnect covered by the solder mask and a metal pad exposed by an opening in the solder mask, as currently claimed in Claim 55.

The Examiner considers that “it would have been obvious to one of ordinary skill in the art at the time of the invention to use a titanium containing layer in the invention of Nozawa because a titanium containing layer is conventionally known in the art layer used as barrier layer or a wetting/adhesion layer on pad.” ~ *See lines 11-14 on page 4 in the last Office Action mailed Dec. 19, 2008* ~

Applicants respectfully traverse the Examiner’s opinion because a titanium-containing layer is not anticipated between Nozawa’s conducting layer 122 and Nozawa’s interconnect layer 120. If the Examiner believes the titanium containing layer is conventionally known, showing an evidence is respectfully requested.

The Examiner considers that “it would have been obvious to one of ordinary skill in the art at the time of the invention to use a nickel-containing layer in the invention of Nozawa because a nickel-containing layer is conventionally known in the art layer used as

barrier layer or a wetting/adhesion layer on pad.” ~ *See lines 17-20 on page 4 in the last Office Action mailed Dec. 19, 2008* ~

Applicants respectfully traverse the Examiner's opinion because a nickel-containing layer is not anticipated between Nozawa's conducting layer 122 and Nozawa's bump 200, but a copper layer 124 is provided between Nozawa's conducting layer 122 and Nozawa's bump 200. ~ *See Fig. 1 and col. 4, lines 65 and 66, in U.S. Pat. No. 6,181,010* ~ If the Examiner believes the nickel-containing layer is conventionally known, showing an evidence is respectfully requested.

The Examiner considers that “it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to protect and strength the package.” ~ *See lines 4-7 on page 5, in the last Office Action mailed Dec. 19, 2008* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is usually used in a chip package with fine-pitched solder bumps to protect the solder bumps. However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any

polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill, formed between a chip and a substrate, enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

Furthermore, the Examiner fails to provide any evidence showing an underfill contacting with a chip and a substrate encloses a copper pillar having a thickness between 10 and 100 micrometers, as currently claimed in Claim 55.

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 55 is respectfully requested.

Applicants respectfully submit independent Claim 55 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 57, 58, 60-62 and 67-68 patently define over the prior art as well.

Response to Claims 69-80

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As previously presented, independent Claim 69 is recited below:

69. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to said second metal pad through an opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a metal layer between said second metal pad and said copper pillar, wherein said metal layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad; and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

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Reconsiderations of Claims 69-80 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 69 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that Nozawa teaches “a substrate [1000] comprising a solder mask [106] and a first pad [104]”. ~ See lines 7-10 on page 3, in the last Office Action mailed Dec. 19, 2008 ~

Applicants respectfully traverse the Examiner's opinion because the element [1000] in Nozawa's device is not a semiconductor chip, but a circuit board. ~ See col. 8, lines 30-44 ~ The elements 106 and 104 are taught not to be arranged on a circuit board, but to be arranged on a semiconductor chip 100. ~ See col. 4, lines 33-39 ~ It is believed that Nozawa fails to disclose that the circuit board 1000 comprises an electrode 104 and an insulating layer 106 that are formed on a semiconductor chip 100.

Furthermore, Nozawa fails to teach, hint or suggest that a substrate has a first side and a second side opposite to the first side, wherein the substrate comprises multiple contact points at the second side, a solder mask at the first side, an interconnect covered by the solder mask and a metal pad exposed by an opening in the solder mask, as currently claimed in Claim 69.

The Examiner considers that “it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to protect and strength the package.” ~ See lines 4-7 on page 5, in the last Office Action mailed Dec. 19, 2008 ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is usually used in a chip package with fine-pitched solder bumps to protect the solder bumps. However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill, formed between a chip and a substrate, enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

Furthermore, the Examiner fails to provide any evidence showing an underfill contacting with a chip and a substrate encloses a copper pillar having a thickness between 10 and 100 micrometers, as currently claimed in Claim 69.

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 69 is respectfully requested.

Applicants respectfully submit independent Claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-80 patently define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Zarneke not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,

A handwritten signature in black ink, appearing to be 'SBA', with a long horizontal flourish extending to the right.

Stephen B. Ackerman, Reg. No. 37,761